Protectli Appliance

Protectli Vault Pro VP6630
2x 10G, 4x 2.5G Intel® i3-1215U

January 13th, 2025

Overview

The Protectli Vault Pro VP6630, features the Intel® Core™ i3-1215U Processor with 4x Intel i226-V 2.5G Network ports and slots for up to 2x Intel X710 10G Network ports. The VP6630 supports up to 64GB DDR5 RAM and includes additional M.2 slots for optional NVMe SSD storage, WiFi, and LTE modules.

Protectli Vaults utilize Intel® components ensuring persistent compatibility with a wide range of operating systems (OS) and applications. The "VP66xx" series Vaults features the same Protectli all-aluminum chassis but with a twist: this series may have a fanless appearance, but they are designed with two additional PWM fans for improved heat dissipation from our highest performing vault series.

Technical Specifications

Model	VP6630
Description	2x 10G, 4x 2.5G Network Port Appliance
Processor	Intel® Core™ i3-1215U (64 bit, Max 4.4 GHz)
Processor Cores	6
Processor Threads	8
Intel® AES-NI	Supported
Virtualization	Intel® Vt-x, Vt-d
Network	2x Intel® X710-BM2 SFP+, 4x Intel® I226-V Ethernet RJ-45
Video / Graphics	Intel® Iris Xe Graphics, 1x HDMI 1.4, 1x DP 1.4a
Audio	Audio over HDMI
Memory	2x SO-DIMM DDR5-4800, Max 64GB
Storage	1x M.2 2280 NVMe
Optional Storage	2x Internal 2.5” SATA 3.0 SSD
External I/O	2x 10G SFP+, 4x 2.5G Ethernet, RJ-45
	1x USB 3.2 Gen 1 Type A, 3x USB 2.0 Type A
	1x USB 3.2 Gen 1 Type C with DisplayPort
	1x RJ-45 COM, 1x USB Type C COM Port
	1x HDMI
	1x DisplayPort 1.4
	1x Nano (4FF) SIM Holder
	6x WiFi/LTE Antenna Mounting Holes
	1x 12V DC Power Jack, Threaded

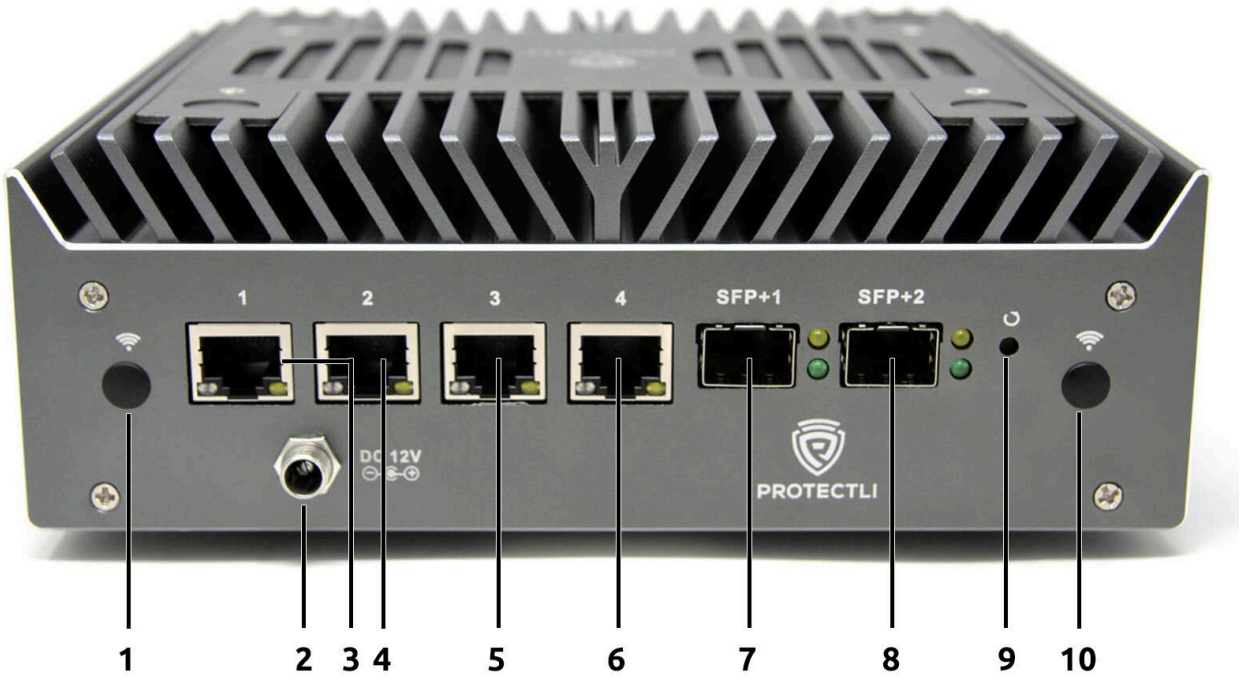
Internal I/O	1x M.2 2280 M-Key PCIe 4.0 x4 (NVMe)
	2x SATA Header, 2x SATA Power
	1x M.2 2230 E-Key PCIe 3.0 x1 for WiFi
	1x M.2 3052 (LTE)
	1x USB 2.0 Header
	1x Trusted Platform Module Header (2x6 pin)
	1x CMOS Reset (2 pin)
	2x PWM Fan Headers (4 pin, 12v)
	1x Front Panel Header (9 pin)
BIOS	AMI® or coreboot
Indicators	1x LED Power Button (Blue), 1x LED Power Indicators (Green), 1x LED Disk Activity Indicator (Yellow), 2x LED Ethernet Activity Indicator (Yellow), 2x LED Ethernet Power Indicators (Green)
Power	Input 12V DC, 1x DC Power Jack, Threaded connector
Power Usage	Idle: 12W, Max: 100W
Chassis	Aluminum, Gray
Chassis Dimensions	7.5 x 7 x 3 in, 191 x 178 x 76 mm
Mounting Options	Desktop, VESA Bracket, Optional 1RU Rack Mount
Weight	5 lbs, 2.3 Kg
Shipping Weight	5 lbs 13 oz, 2.6 Kg
Operating Temperature	+14° - +122° F, -10° - +50° C
Operating Humidity	0 – 95% relative humidity, non-condensing
Approvals	UL (Power Supply), FCC Part 15 Class B, CE, RoHS
Country of Origin	Made in China, Assembled in USA, Canada, or Germany
Optional WiFi	1x M.2 2230 E-Key PCIe 802.11ac/a/b/g/n (PCIe)
Optional LTE Cellular	1x M.2 3052 B-Key USB 3.2 Gen 1 (LTE), with Nano (4FF) SIM holder
Optional TPM	1x Trusted Platform Module, TPM 2.0

Included Accessories and Components

120W Power Supply with barrel connector
US/CA Power Cable *(Other regional power cables available)*
USB Type-C (with Type-A adapter) to USB Type-C Serial Console Cable
8x SSD mounting screws
2x SATA power cables
2x SATA data cables
Heat sink with thermal pad and mounting hardware
4x M2 screws
VESA Bracket mount with hardware
Quick Start Guide

External Interfaces

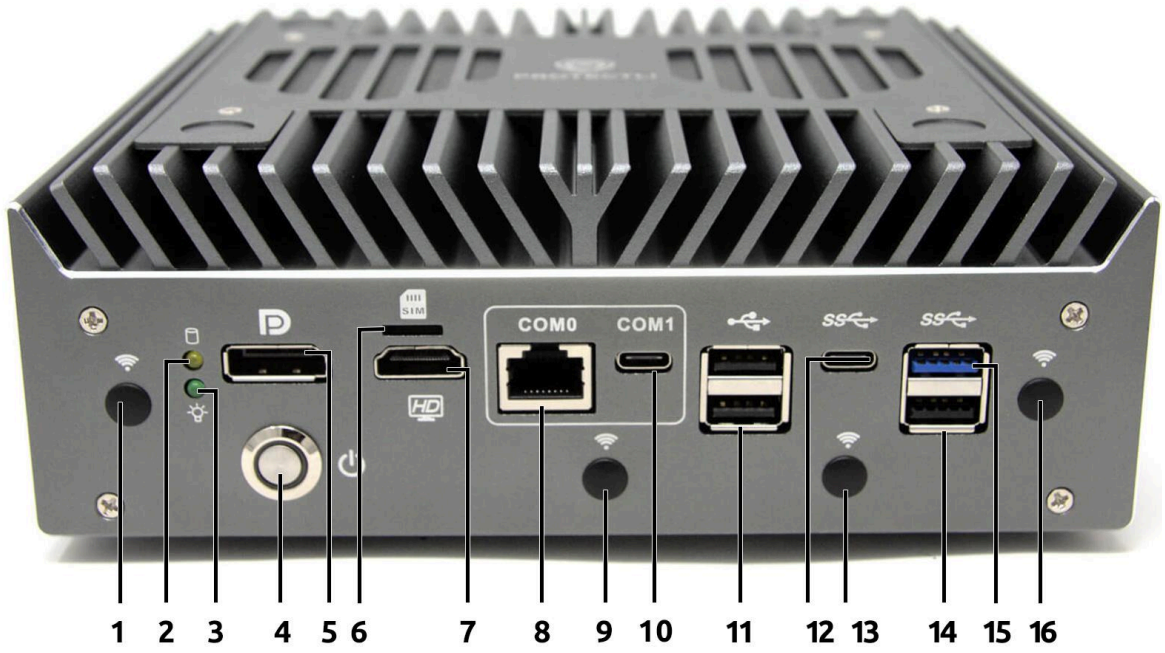
Front Panel Configuration



Item #	Object	Label	Description
1, 10	Antenna Ports		Two antenna ports for adding radio antennas (WiFi, LTE, etc.). The ports are covered by plugs while not in use.
2	Power Supply Connector	DC 12V	12V DC threaded barrel connector for the 120W external power supply. Positive rail is the tip, negative is sleeve. Barrel dimensions: 5.5mm x 2.5mm
3	Ethernet Port 1	1	10/100/1000/2500 Mbps Intel® i226-V ethernet port. [Left LED will illuminate Amber at 2500Mbps, Green at 1000Mbps, and will be turned off when connected at 100/10Mbps]
4	Ethernet Port 2	2	10/100/1000/2500 Mbps Intel® i226-V ethernet port.

			[Left LED will illuminate Amber at 2500Mbps, Green at 1000Mbps, and will be turned off when connected at 100/10Mbps]
5	Ethernet Port 3	3	10/100/1000/2500 Mbps Intel® i226-V ethernet port. [Left LED will illuminate Amber at 2500Mbps, Green at 1000Mbps, and will be turned off when connected at 100/10Mbps]
6	Ethernet Port 4	4	10/100/1000/2500 Mbps Intel® i226-V ethernet port. [Left LED will illuminate Amber at 2500Mbps, Green at 1000Mbps, and will be turned off when connected at 100/10Mbps]
7	SFP+ Port 1	SFP+ 1	Intel X710-BM2 10/1GbE SFP+ port. [Top LED will illuminate Orange at 10GbE, LED will be off when at 1GbE]
8	SFP+ Port 2	SFP+ 2	Intel X710-BM2 10/1GbE SFP+ port. [Top LED will illuminate Orange at 10GbE, LED will be off when at 1GbE]
9	Reset Button (recessed)		A momentary switch connected to internal jumpers on the motherboard (see label RSTSW1). Depending on the jumper configuration, this button may perform as either an ACPI Reset or a GPIO button that can be programmed in an OS. For GPIO mode, the implementation is undefined, and may be polled using I2C or ISA registry examination. In Linux, the ISA address 0x0A00 will return 42 when the button is pressed in GPIO mode, 46 when not pressed in GPIO mode. The register will always read 46 if the device is in ACPI Reset mode, as the button's operation is now undefined for GPIO purposes.

Rear Panel Configuration



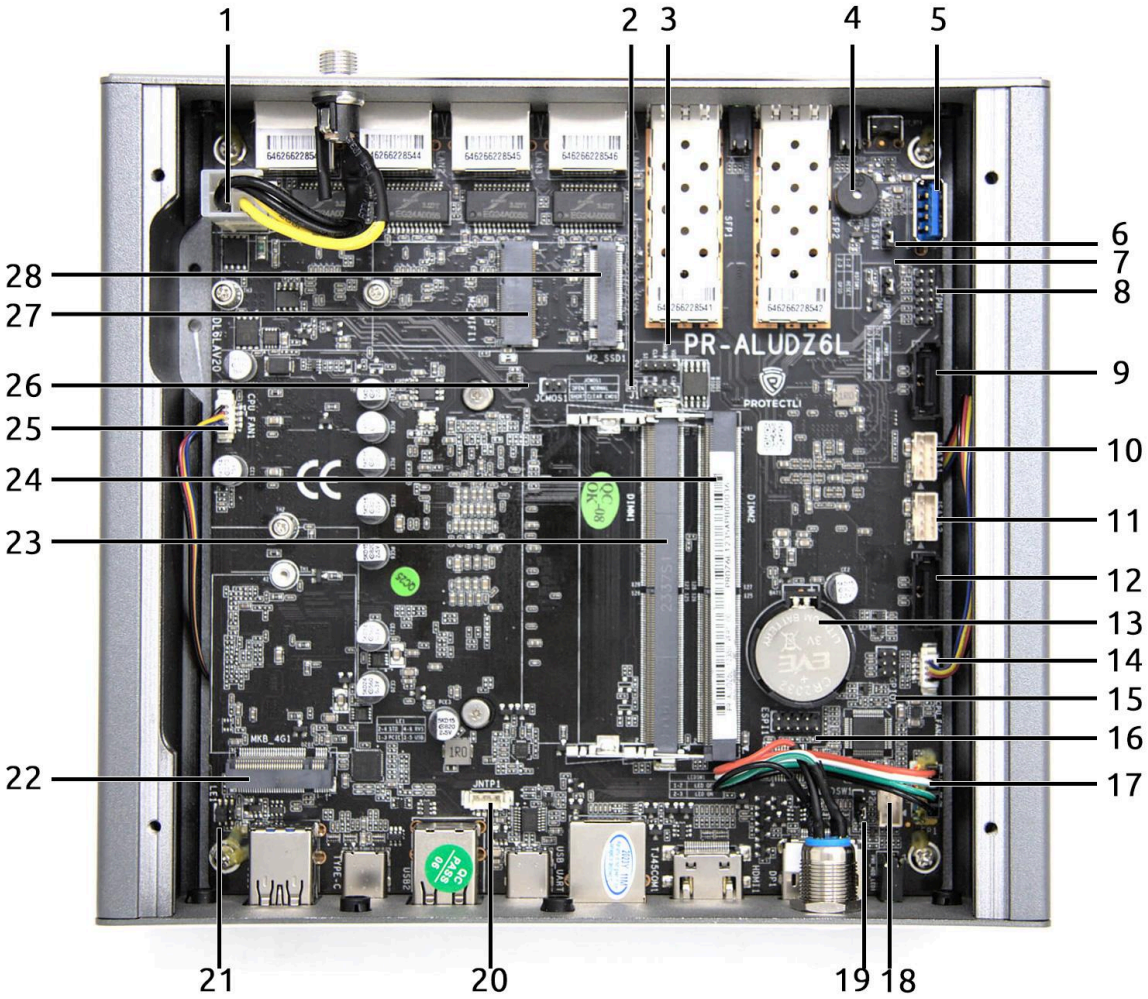
Item #	Object	Label	Description
1, 9, 13, 16	Antenna Ports		Four antenna ports for adding radio antennas (WiFi, LTE, etc.). The ports are covered by plugs while not in use.
2	HDD Activity LED		LED emits amber when data activity is detected on an NVMe interface.
3	Power Indicator LED		LED emits solid green when the device is powered on.
4	Power Button		Pressing the power Button will power the unit on and illuminate with a blue LED. *In OSes configured to handle ACPI signals, pressing the power button initiates a shutdown.* *Pressing and holding the Power Button for 5 seconds will force the unit to power off.*
5	DisplayPort Connector		Video and audio output via DisplayPort.

6	SIM Slot		Nano (4FF) SIM slot for providing a SIM card to an optional internal cellular modem.
7	HDMI Connector		Video and audio output via HDMI.
8	Serial Console Port	COM0	RS-232 serial communications via RJ-45. Default port settings: ● 115200 baud ● No parity ● 8 databits ● 1 stopbit AMI firmware will prioritize this over the USB-C Console Port
10	Serial Console Port	COM1	RS-232 serial communications via FTDI FT230XS UART, exposed through USB 3.2 Gen 1 Type C connector. Default port settings: ● 115200 baud ● No parity ● 8 databits ● 1 stopbit AMI firmware will prioritize the RJ45 Console Port. To change this, follow the instructions here: https://kb.protectli.com/kb/com-port-tutorial/#articleTOC_11
11	USB2 Connectors		Two USB 2.0 Type-A connectors.
12	USB-C Connector		USB 3.2 Gen 2† Type-C connector with DisplayPort
14	USB Connector		USB 2.0 Type-A connector.
15	USB Connector		USB 3.2 Gen 2† Type-A connector.

†USB-IF naming standard for USB transfer rates: "USB 3.2 Gen 2" is the equivalent and current name for "USB 3.1 Gen 2" offering a theoretical maximum speed of 10 Gigabits (~1.2GB) per second. Older kernels and operating systems may not report the most recent naming convention. For a full linguistic deep dive, please see 3.1 and 3.2 Specification Language Usage Guidelines from USB-IF.
https://www.usb.org/sites/default/files/usb_3_2_language_product_and_packaging_guidelines_final.pdf,
https://www.usb.org/sites/default/files/usb_3_1_language_product_and_packaging_guidelines_final_0.pdf

Internal Interfaces

Motherboard Layout and Pin Configuration



Item #	Object	Label	Description
1	DC IN	DC_IN1	2x2 Molex for +12VDC power.
2	BIOS Programming Headers	J1	One half of BIOS chip jumpers for external programming. 1. VOD 2. HOLD# 3. CLK 4. SI

<table>
<tr><td>3</td><td>BIOS Programming Headers</td><td>J2</td><td>One half of BIOS chip jumpers for external programming.
1. CS#
2. SO
3. WP#
4. GND</td></tr>
<tr><td>4</td><td>Buzzer</td><td>BUZZ1</td><td>PC speaker.</td></tr>
<tr><td>5</td><td>USB3</td><td>USB3</td><td>Internal USB 3.2 Gen 2 Type-A connector. (Theoretical maximum throughput of 10 Gigabits [~1.2GB] per second)</td></tr>
<tr><td>6</td><td>Reset Button Function Jumper</td><td>RSTSW1</td><td>Jumper setting determines the functionality of the Reset Button (Front Features, #9) as well as the associated pins on FP1 (Motherboard Top View, #17).
● Tied Pins 1-2: ACPI Reset
● Tied Pins 2-3: GPIO (Default)</td></tr>
<tr><td>7</td><td>Power Restore Jumper</td><td>JPWR1</td><td>Jumper setting determines system state after power is restored after experiencing power loss.
● Tied Pins 1-2: Remain powered off
● Tied Pins 2-3: Automatic power on (Default)

In order for this behavior to work, you must also change a setting in the AMI firmware menu. Navigate to Advanced>ACPI Config and set Restore ON Power Loss to “Pch Control”.

The jumper location will not affect the automatic power on function when coreboot 0.9.0 firmware is utilized. It will always be enabled.</td></tr>
<tr><td>8</td><td>TPM</td><td>JTPM1</td><td>Trusted Platform Module header for a TPM2.0 hardware device. (2x6, 2.0mm pitch)

<table><tr><td>Pin 1: VDD</td><td>Pin 2: TPM_CS#</td></tr><tr><td>Pin 3: SPI_MISO</td><td>Pin 4: SPI_MOSI</td></tr><tr><td>Pin 5: NC1</td><td>Pin 6: SPI_CLK</td></tr><tr><td>Pin 7: GND</td><td>Pin 8: SPI_REST</td></tr><tr><td>Pin 9: NC2</td><td>X</td></tr><tr><td>Pin 11: NC3</td><td>Pin 12: TPM_PIRQ#</td></tr></table></td></tr>
<tr><td>9</td><td>SATA Data Connector</td><td>SATA1</td><td>SATA III data connector. Recommended for additional storage, such as a 2.5” SATA SSD. (Standard 7-PIN SATA III Plug)</td></tr>
</table>

<table>
<tr><td>10</td><td>SATA Power Connector</td><td>JSATA1</td><td>SATA power connector for additional storage. (1x4, 2.0mm pitch, JST PH style connector)</td></tr>
<tr><td>11</td><td>SATA Data Connector</td><td>JSATA2</td><td>SATA power connector for additional storage. (1x4, 2.0mm pitch, JST PH style connector)</td></tr>
<tr><td>12</td><td>SATA Power Connector</td><td>SATA2</td><td>SATA III data connector. Recommended for additional storage, such as a 2.5” SATA SSD. (Standard 7-PIN SATA III Plug)</td></tr>
<tr><td>13</td><td>CMOS Battery</td><td>BAT1</td><td>3V CR2032.</td></tr>
<tr><td>14</td><td>CPU Fan Header</td><td>CPU_FAN2</td><td>Four-pin PicoBlade-compatible header (1.25mm pitch) for included PWM CPU fan located on chassis. The connected fan is 60x60x10MM.</td></tr>
<tr><td>15</td><td>GPIO</td><td>GPIO1</td><td>General Purpose I/O header. (2x3, 2.0mm pitch) The column containing Pin 1 is the one closest to the CMOS battery.<table><tr><td>Pin 1: +5V</td><td>Pin 2: GND</td></tr><tr><td>Pin 3: GPIO 56</td><td>Pin 4: GPIO 57</td></tr><tr><td>Pin 5: GPIO 60</td><td>Pin 6: GPIO 61</td></tr></table>AMI firmware allows for the ability to change the 4 GPIO pins between “low”, “high”, and “input” voltage settings. Low setting registers at 0.0014V and high setting registers at 5.10V. (These settings are found at Advanced>IT8659 Super IO Config>GPIO Config)</td></tr>
<tr><td>16</td><td>ESPI</td><td>ESPI1</td><td>eSPI header for BIOS chip flashing.</td></tr>
</table>

<table>
<tr>
<td>17</td>
<td>Front Panel Header</td>
<td>FP1</td>
<td>Internal header for adding external device controls and indicators featured through the front panel, such as power button, reset button, activity LEDs, etc. (2x5, 2.54mm pitch) The included power button will be connected to pins 2, 4, 6, and 8. The pinout chart below has been colored to match the baseboard.

<table>
<tr><td>Pin 1: HDD_LED+ [+3.3V]</td><td>Pin 2: PWR_LED+ [+5V]</td></tr>
<tr><td>Pin 3: :SSD_LED-</td><td>Pin 4: PWR_LED-</td></tr>
<tr><td>Pin 5: RST_GND</td><td>Pin 6: PW_ON</td></tr>
<tr><td>Pin 7: RST</td><td>Pin 8: PWON_GND</td></tr>
<tr><td>Pin 9: No connection</td><td>X</td></tr>
</table>
</td>
</tr>
<tr>
<td>18</td>
<td>Front Panel Header</td>
<td>FP2</td>
<td>Additional headers for “Front-Panel-like” control. These pins could be used by an auxiliary device to power on, power off, and monitor unit power state.

Pin 1 is located closest to the CMOS battery (#13).

<table>
<tr><td>Pin 1: LED +</td><td>Pin 2: LED -</td><td>Pin 3: Power -</td><td>Pin 4: Power +</td></tr>
</table>

Monitoring pins 1 and 2 will dictate if the unit is powered on. Measurement between 1VDC and 3.5VDC indicated the unit is on (S0), 0VDC is powered off (S5).

Shorting pins 3 and 4 will emulate an ACPI power button.

Shorting the connection for any duration will send an ACPI command to either power on (S0) if in a powered-off state, or as an ACPI_SHUTDOWN event to be handled by the OS.
Shorting the connection for over 5 seconds will force the system to enter a soft-off state (S5).

The included “SSD Cable Kit” for mounting an additional 2.5” SSD contains a power cable that can be repurposed into a breakout connector as the FP2 and JSATA1/JSATA2 (#10 and #12 respectively) are the same connector size.
</td>
</tr>
</table>

<table>
<tr><td>19</td><td>LED Control Jumper</td><td>LEDSW1</td><td>Jumper setting determines the operation of chassis LEDs. This will only affect the LED behavior of devices connected to FP2.

● Tied Pins 1-2: LEDs Off
● Tied Pins 2-3: LEDs On (Default)</td></tr>
<tr><td>20</td><td>External Time Header</td><td>JNTP1</td><td>Header for use with an external time device, such as a GPS receiver. Serial data is processed by the TPS65994AD Dual Port USB Type-C® and USB PD Controller by way of a slave I²C interface.

1. Serial data
2. Serial clock
3. +5 VDC
4. GND</td></tr>
<tr><td>21</td><td>Lane Configuration</td><td>LE1</td><td>Jumper setting determines the operation mode of MKB_4G1 (#22). Two jumpers are included and will dictate the mode.

One jumper is used to configure the operation mode:

● Jumped Pins 1-3: PCIe Mode
● Jumped Pins 3-5: USB 3.2 Mode

One jumper is used to configure voltage settings defined for vendor-reserved use cases. Such examples include specific M.2 modules that require voltages to be present on certain pins to modify the operation mode of the M.2 module itself.

● Jumped Pins 2-4: No voltage at pins 20 and 22.
● Jumped Pins 4-6: 1.83V at pin 20 and 3.3V at pin 22.

Factory default setting is to jump pins 1-3 and 2-4, placing the MKB_4G1 (#22) M.2 port in a standard PCIe Mode.

The following table maps the pins in the same orientation of the photo above. Pin 1 is indicated by a white arrow printed on the motherboard.

<table><tr><td>Pin 2</td><td>Pin 4</td><td>Pin 6</td></tr><tr><td>Pin 1</td><td>Pin 3</td><td>Pin 5</td></tr></table></td></tr>
</table>

22	LTE Expansion Slot	MKB_4G1	Connector uses the designated protocol based on the LE1 Jumper (#21) via an m.2 3052 B-Key. Designed for Protectli cellular modems, but is not limited in its capabilities.
23	Memory Slot	DIMM1	DDR5 SODIMM.
24	Memory Slot	DIMM2	DDR5 SODIMM.
25	CPU Fan Header	CPU_FAN1	Four-pin PicoBlade-compatible header (1.25mm pitch) for included PWM CPU fan located on chassis. The connected fan is 60x60x10MM.
26	NVRAM Reset Jumper	JCMOS1	Shorting this jumper while the CMOS battery is connected will reset the BIOS NVRAM.
27	WiFi Expansion Slot	M2_WIFI1	Connector uses PCIe 3.0 x1 protocol over an M.2 E-Key socket. Designed for Protectli WiFI modules, but is not limited in its capabilities.
28	M.2 NVMe Connector	M2_SSD1	Connector uses PCIe 4.0 x4 protocol over an M.2 M-Key socket. It is designed for an NVMe storage device, but is otherwise a functional PCIe port.

Dimension View

Document History

2025-01-13

- Removed duplicate data from motherboard view table

2025-01-03

- Added “Overview” section
- Added “Included Accessories” section
- Updated section headers for clarity
- Added info about LED behavior for NICs
- Added audio output to DisplayPort capabilities
- Added info about Console redirection prioritizing the RJ45 port
- Changed CPU Fan Header to 2x instead of 1x, added pitch size
- Added pitch size of Trusted Platform Module header
- Removed mention of non-existing USB 2.0 Header and changed to USB 3.2 Gen 2 Type A Port
- Added pitch size for Front Panel Header
- Added USB naming convention notes under "rear features"
- Added pin layout for GPIO header, pitch size, and included information regarding firmware settings with AMI
- Added pin layout for TPM header, pitch size
- Added note to Power Restore Jumper regarding behavior with coreboot and how to configure it with AMI
- Added size of fan in the CPU fan header section as well as pitch of header
- Added FP1 layout, pitch size, and note regarding the fact the power button is connected to this header by default
- Added pitch size and connector type for SATA1 & 2 header
- Added plug type for JSATA1 and 2
- Corrected JSATA2 and SATA2 being improperly labeled as they were swapped
- Added note to LEDSW1 regarding the behavior only affects FP2 and removed mention of it affecting the built in LEDs
- Removed mention of "Designed for Protectli WiFi" on LTE Expansion Slot, reworded to only include Protectli Cellular Modems
- Added note for theoretical speeds for USB3

2024-10-24

- Corrected USB port version and generations listed in “Specifications” and “Front Features” sections
- Clarification of wording throughout the “System Features” section
- Corrected LED colors
- Corrected number of LED indicators for 10G ethernet from 1 to 2
- Corrected BIOS options to include coreboot
- Corrected number of Processor Cores from 10 to 6
- Corrected number of Processor Threads from 12 to 8

2024-08-28

- Corrected PCIe specification

2024-08-01

- Changed “PC Speaker” to “PC speaker”
- Changed ”RS232” to “RS-232”
- Updated linked spec sheet with ® and ™ as necessary for Intel and AMI
- Changed linked spec sheet from “i226V” to “i226-V”
- Updated linked spec sheet from “4FF SIM” to “Nano (4FF) SIM”

2024-06-28

- Clarified PCI and USB specifications such as speed, protocol, etc.

2024-05-16

- Added additional details regarding the serial port FTDI driver.
- Added details about the Intel X710 SFP+ chipset.
- Added details about how RSTSW1 operation modes affect Front Panel item #9: “Reset Button (recessed)”
- Clarified LTE and/or WiFi slot naming schemes
- Clarified threading on barrel connector
- Updated FP2 (#18 Motherboard View) connector properties and pinout information

2024-04-29

- Initial document